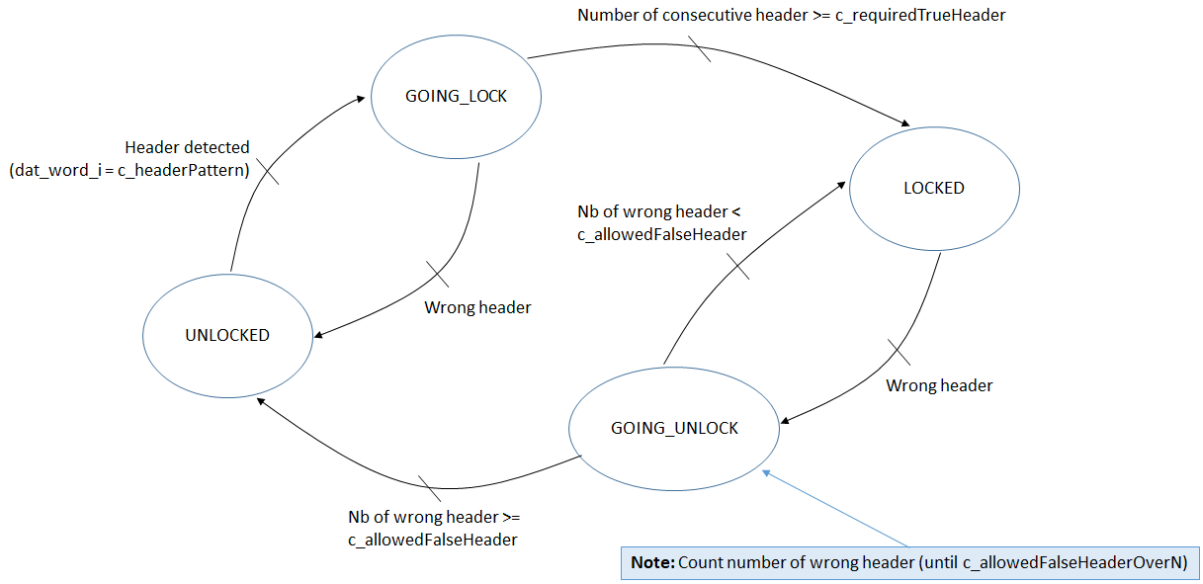
LpGBT-FPGA: How to configure the frame aligner.

The frame aligner is implemented close to the transceiver to align the received data and place the header on the first bits of the frame. Therefore, it is made of a pattern searcher and a bitslip controller state machine to check the position and request a shift when required. According to the LpGBT specification, the uplink's header is fixed regardless of the way the modules are configured (FEC5 or FEC12 and 10.24 or 5.12Gbps).

Locking state machine

The locking state machine looks for the header and computes statistics to check whether the frame is locked or not. This statistics allows remaining locked even when a random error is detected (depends on the B.E.R – The header is out of the FEC loop).



Note: The frame aligned tolerance can be adjusted by the user with the generic parameter available on top of the entity.

Fixed latency

In order to ensure a fixed latency, a signal is toggled every time a shift of the frame is requested. Indeed, because of the Dual Data Rate mode of the transceiver, the clock is shifted every other request. On the second request, only the data are shifted. However, because the clock shall be aligned always on the same phase, the number of request count parity shall always be the same.

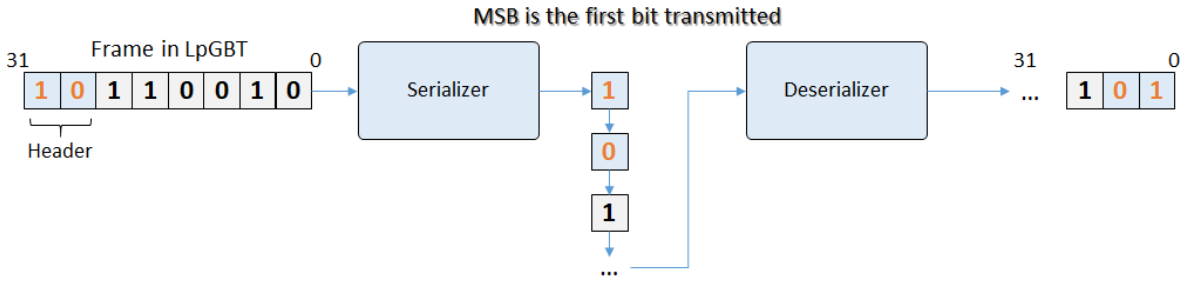
Instead of counting the number of request and triggering the reset signal of the transceiver when it is odd or even depending on the configuration, the pattern search module is just toggling a signal and checks whether its value is '1' or '0'.

To simplify the locking state machine, when the constant phase is not required, or when an accuracy of 1UI is acceptable, this feature can be disabled by setting the c_resetOnEven parameter to 0 (1 to enable). Finally, when enabled, the reset duration is counted in freeRunningClock periods and it can be fixed using the c_resetDuration generic value.

How to connect the dat_word_i input

The dat_word_i input signal shall be connected to a bus containing the header as it is expected and described on the c_headerPattern parameter. Therefore, this signal must be constructed before

being connected to the frame aligner according to the LpGBT specification (word inversion and interleaving). For example, in FEC12 / 10.24Gbps mode, the header is “10” and it is not interleaved, meaning that the expected pattern is “01” on bit (1 downto 0) from the MGT word.



Therefore, depending on the SerDes configuration (static 5.12Gbps, static 10.24Gbps or Dynamic), the frame aligner parameters take different values. In dynamic mode, with an oversampling ratio of 2, the header shall be aligned using 4bit instead of 2 with each bit duplicated as shown below:

Data rate 5.12 or 10.24Gbps:

```
dat_word_i      <= upLinkWord_from_mgt_s(1 downto 0);
c_headerPattern <= “01”;
```

Data rate dynamic in 5.12Gbps mode:

```
dat_word_i      <= upLinkWord_from_mgt_s(3 downto 0);
c_headerPattern <= “0011”;
```